LISTING OF CLAIMS

Claims 1-10 (Canceled).

11. (Original). A system for time ordering events comprising:

a plurality of functional circuit modules, each functional circuit module being clocked by a clock that represents a different time domain and having timestamping circuitry, the timestamping circuitry providing a message that indicates a point in time when a predetermined event occurs; and

an interface module coupled to each of the plurality of functional circuit modules, the interface module providing control information to the plurality of functional circuit modules to indicate at least one operating condition that triggers the predetermined event, the interface module receiving at least one timestamping message from a first time domain when the predetermined event occurs in one of a plurality of time domains including the first time domain.

12. (Original) The system of claim 11 wherein the interface module further comprises:

storage circuitry for storing the control information as programmable control information that determines the at least one operating condition that triggers the predetermined event.

13. (Original) The system of claim 12 wherein the at least one operating condition that triggers the predetermined event further comprises at least one of: entrance into or exit from a power mode of operation, a change in source of a clock, a change in clock periodicity, a predetermined change in a hardware counter value, entry into and exit from a debug mode of operation, and occurrence of at least one user programmable event.

14. (Original) The system of claim 11 wherein the timestamping circuitry further comprises:

a counter for determining either absolute or relative time in a corresponding functional circuit module;

time domain identification circuitry for providing a time domain identifier; and

clock status circuitry for providing one or more operating characteristics of a clock in the corresponding functional circuit module.

15. (Original) The system of claim 14 wherein the timestamping circuitry further comprises circuitry for generating a code to be included in each message to identify a format of information included in a corresponding message.

16. (Original) The system of claim 14 wherein the interface module further comprises an arbiter having circuitry for generating a code to be included in each timestamping message to identify a format of information included in a corresponding timestamping message.

17. (Original) The system of claim 11 wherein the message provided by at least one of the plurality of functional circuit modules has a format that comprises at least a time count value that is an absolute value referenced to a known starting value, status information of a clock signal associated with one of the functional circuit modules, and an identifier that indicates a corresponding time domain associated with the timestamping message.

18. (Original) The system of claim 17 wherein the message has a format that further comprises a field that identifies that the format of the timestamping message has an absolute value time count value.

19. (Original) The system of claim 11 wherein the message provided by at least one of the plurality of functional circuit modules has a format that comprises at least a time count value that is a relative value referenced to a last occurring predetermined event, status information of a clock signal associated with one of the functional circuit modules, and an identifier that indicates a corresponding time domain associated with the timestamping message.

20. (Original) The system of claim 19 wherein the message has a format that further comprises a field that identifies that the format of the timestamping message having a relative value time count value.

21. (Original) The system of claim 11 wherein the timestamping message has a format that comprises a time count value corresponding to each of the functional circuit modules and predetermined status information associated with each of the functional circuit modules when the predetermined event occurs.

22. (Original) The system of claim 11 wherein the control information is programmable.

23. (Original) The system of claim 11 wherein the interface module further comprises:

at least one register for storing the control information.

24. (Original) The system of claim 11 wherein the interface module provides timestamping messages from all time domains at a common interface port.

25. (Original) The system of claim 24 wherein the common interface port of the interface module meets IEEE ISTO 5001 (NEXUS) compliance.

26. (Original) A system for time ordering events comprising:

a plurality of functional circuit module means, each being clocked by a clock that represents a different time domain and having timestamping circuit means, the timestamping circuit means providing a message that indicates a point in time when a predetermined event occurs; and

interface module means coupled to each of the plurality of functional circuit module means, the interface module means providing control information to the plurality of functional circuit module means to indicate at least one operating condition that triggers the predetermined event, the interface

module means receiving at least one timestamping message from a first time domain when the predetermined event occurs in one of a plurality of time domains including the first time domain.

27. (Original) The system of claim 26 wherein the timestamping messages from all time domains are provided by interface module means at a common interface port means.

28. (Original) A system comprising:

a plurality of functional circuit modules on a same integrated circuit, each functional circuit module being clocked by a clock that represents a different time domain, and each functional module having timestamping circuitry operating at independent clock rates for providing timestamp messages.

29. (Original) The system of claim 28 wherein the timestamp messages each indicate a point in time when a predetermined event occurs.

30. (Original) The system of claim 29 further comprising:

an interface module coupled to each of the plurality of functional circuit modules, the interface module providing control information to the plurality of functional circuit modules to indicate at least one operating condition that triggers the predetermined event, the interface module receiving at least one timestamping message from a first time domain when the predetermined event occurs in one of a plurality of time domains including the first time domain.

31. (Original) A method of reconstructing time ordering of events that occur in multiple time domains in a system, the method comprising:

receiving multiple timestamping messages in one of an ordered time sequence and an unordered time sequence;

tracking relative count values of multiple time domain counters associated with the multiple time domains and operating at independent clock rates; and

sorting debug information in time ordered sequence, the debug information being associated with a timestamp provided from one of the multiple time domains.

32. (Original) The method of claim 31 further comprising providing the debug information via a debug message.

33. (Original) The method of claim 32 further comprising implementing the debug messages as at least one of a program trace message, a data trace message and a watchpoint message.

34. (Original) The method of claim 31 further comprising generating the multiple timestamp messages by:

providing control information corresponding to each of multiple time domains, the control information indicating when a timestamp message for each of the multiple time domains is to be generated;

determining when a time domain event that requires generation of a timestamp message occurs in any one of the multiple time domains; and

generating a timestamp message corresponding to a predetermined one of the multiple time domains in response to determining that the time domain event occurred.

35. – 45. (Canceled).